EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"20050172182"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/03/13 11:55
L2	25077176	@ad<"20040115"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L3	2	"20050172182"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L4	307820	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L5	111395	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) And (semi$1conduct$4 substrate die dice)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L6	6141	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) And (semi$1conduct$4 substrate die dice) And (((error mistake fail$4 false flaw test$4) with (result$3 report$3 list$3 data record$4 document$6 descript$6 history)) same ((voltage power v vs) same (optim$7 operat$3 best)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41

EAST Search History

L7	4234	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) And (semi$1conduct$4 substrate die dice) And (((error mistake fail$4 false flaw test$4) with (result$3 report$3 list$3 data record$4 document$6 descript$6 history)) same ((volt$3 power v vs) with (level limit threshold range amount)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L8	2034	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) And (semi$1conduct$4 substrate die dice) And (((error mistake fail$4 false flaw test$4) with (result$3 report$3 list$3 data record$4 document$6 descript$6 history)) with ((volt$3 power v vs) with (level limit threshold range amount)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L9	1681	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) And (semi$1conduct$4 substrate die dice) And (((error mistake fail$4 false flaw test$4) with (result$3 report$3 list$3 data record$4 document$6 descript$6 history)) with ((volt$3 power v vs) with (level limit threshold range amount))) And ((optim$7 operat$3 ideal$5 model "most adj favorable" advantage$5) with (volt$3 v vs power))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41

EAST Search History

L10	851	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) And (semi$1conduct$4 substrate die dice) And (((error mistake fail$4 false flaw test$4) near8 (result$3 report$3 list$3 data record$4 document$6 descript$6 history)) with ((volt$3 power v vs) near7 (level limit threshold range amount))) And ((optim$7 operat$3 ideal$5 model "most adj favorable" advantage$5) near5 (volt$3 v vs power))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L11	556	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) And (semi$1conduct$4 substrate die dice) And (((error mistake fail$4 false flaw test$4) near5 (result$3 report$3 list$3 data record$4 document$6 descript$6 history)) with ((volt$3 power v vs) near3 (level limit threshold range amount))) And ((optim$7 operat$3 ideal$5 model "most adj favorable" advantage$5) near3 (volt$3 v vs power))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L12	155	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) And (semi$1conduct$4 substrate die dice) And (((error mistake fail$4 false flaw test$4) near2 (result$3 report$3 list$3 data record$4 document$6 descript$6 history)) with ((volt$3 power v vs) near2 (level limit threshold range amount))) And ((optim$7 operat$3 ideal$5 model "most adj favorable" advantage$5) near2 (volt$3 v vs))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41

EAST Search History

L13	114935	L2 and ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) with voltage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L14	16991	L2 and ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) with voltage) And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L15	4105	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) and ((test$4 verif$7 check$4) with ((volt$3) near2 (level)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L16	216	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) and ((test$4 verif$7 check$4) with ((volt$3) near2 (level))) and (optim$7 near3 volt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 13:46
L17	105	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) and ((test$4 verif$7 check$4) near4 ((volt$3) near2 (level))) and (optim$7 near3 volt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L18	131	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4 simulat$4 synthes$5 satisf$5) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) and ((test$4 verif$7 check$4) near4 wafer) and (optim$7 near3 volt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41

EAST Search History

L19	61	L2 And ((test$4 verif$7 drc (design$4 adj L3 check$4) check$4) same (processor chip ic (integrated adj circuit) cpu mpu (micro$1processor$3))) and ((test$4 verif$7 check$4) same (processor chip wafer ic (integrated adj circuit) cpu mpu (micro$1processor$3)) same ((multiple different many various) near4 volt$3)) and (optim$7 near3 volt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L20	767	L2 and ((change multiple differ$5 many various) near2 volt$4) with (((error mistake fail$4 false flaw test$4) near3 (result$3 report$3 list$3 data record$4 document$6 descript$6 history)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L21	259	L2 and ((vary change multiple differ$5 many various) near volt$4) with (((error mistake fail$4 false flaw test$4) near (result$3 report$3 list$3 data record$4 document$6 descript$6 history)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L22	8	L2 and ((vary change multiple differ$5 many various) near volt$4) with (((error mistake fail$4 false flaw test$4) near (result$3 report$3 list$3 data record$4 document$6 descript$6 history))) and (optim$7 near2 volt$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L23	218	L2 and ((volt$4)) with (((error mistake fail$4 false flaw test$4) near (result$3 report$3 list$3 data record$4 document$6 descript$6 history))) and (optim$7 near2 volt$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L24	44	L2 and (test) same (wafer ic processor chip) same ((change multiple differ$5 many vary various other) near2 volt$4) And (optim$7 near2 volt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L25	16	L2 and ((test$4 verif$6 check$4) with (wafer ic processor chip)) with ((change multiple differ$5 many vary various other) near2 volt$4) And (optim$7 near2 volt$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41

EAST Search History

L26	2287	L2 and ((test) same (wafer ic processor chip) same ((level limit threshold range amount) near2 volt$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L27	691	L2 and ((test) with (wafer ic processor chip) with ((level limit threshold range amount) near2 volt$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L28	248	L2 and (((test) near2 (wafer ic processor chip)) with ((level limit threshold range amount) near2 volt$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L29	215	L2 and (((test) near2 (wafer ic processor chip)) with ((level limit threshold range amount) near volt$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L30	496	L2 And (((error mistake fail$4 flaw) near2 (test$3 result$3 report$3 list$4 data)) with (volt$4 near2 level))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L31	37	L2 And (((error mistake fail$4 flaw) near2 (test$3 result$3 report$3 list$4 data)) with ((change multiple many various vary differ$4) near2 (volt$4 near2 level)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L32	13	(US-20040111231-$ or US-20040128567-$ or US-20040128566-$ or US-20030042970-$ or US-20050071094-$ or US-20040125711-$ or US-20020085469-$ or US-20040082086-$ or US-20040004888-$).did. or (US-5457695-$ or US-5648766-$ or US-6574463-$).did. or (EP-305987-$).did.	US-PGPUB; USPAT; DERWENT	OR	ON	2006/03/13 10:41

EAST Search History

L33	2	"20020131531"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 10:41
L34	0	"20040111231" and perl	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2006/03/13 13:38
L35	370	l2 and ((Perl) with (advantag$4 benefit better known conventional))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 13:50
L36	1	l2 and ((Perl) with (advantag$4 benefit better known conventional) with calculat$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 13:52
L37	15	l2 and ((Perl) with (advantag$4 benefit better known conventional) with pars$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/13 13:54